REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-6 and 8 under 35 USC § 103 (a) as being unpatentable over Matsunaga (U.S. Patent No. 6,759,906) in view of Aubauer (U.S. Patent Application No. US2005/0276423) and claims 7 and 9-14 under 35 USC § 103 (a) as being unpatentable over Matsunaga (U.S. Patent No. 6,759,906) in view of Aubauer (U.S. Patent Application No. US2005/0276423) and Melo (U.S. Patent No. 6,243,817). The rejections and objections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-14.

2. Claims 1-6 and 8 have been rejected under 35 USC § 103 (a) as being unpatentable over Matsunaga (U.S. Patent No. 6,759,906) in view of Aubauer (U.S. Patent Application No. US2005/0276423). The applicant respectfully disagrees with this rejection and the reasoning thereof. In addition to the arguments made in the response to the office action mailed on 1/11/07, the applicant states the following.

In support of the above mentioned rejection the Examiner stated that Figure 26 is the whole integrated circuit of microphone input 323. The applicant respectfully disagrees. Matsunaga teaches at column 16, lines 49-50, that Figure 26 shows a block diagram of the whole portable telephone. Matsunaga further teaches at column 16, lines 52-65, that the portable telephone includes a voice microphone 323, a voice interface 330, a DSP 351 for processing voice and sending/receiving signals, an application specific integrated circuit 352, and other components. As such, Figure 26 is not a diagram of an integrated circuit, but a diagram of a telephone that includes integrated circuits (e.g., ASIC 352).

In addition, the Examiner stated that Figure 1 of Matsunaga discloses a first IC pin with corresponding text at column 8, lines 49-54. However, a review of this text and the preceding text reveals that the high frequency power amplifier 100 includes Q1-Q3 connected sequentially in a cascaded manner. Transistor Q3 in the last stage is composed of discrete parts while Q2 and Q3 (which appears to be a typographical error and should

be Q1) in the middle and initial states are assembled into a semiconductor integrated circuit. As such, the power amplifier includes discrete components for Q3 and an IC for Q1 and Q2. No matter how broadly the present claim is interpreted, a power amplifier having discrete components and an IC is not equivalent to an IC pin.

The Examiner further supports the present rejection by stated that a first resistor is shown in Figure 1 and a return voltage is represented by a vg1, which is a gate bias voltage. The applicant agrees that Figure 1 of Matsunaga includes a resistor R1, however, the resistor is not coupled to an IC and to a return voltage as is claimed. As shown in Figure 1, resistor R1 is coupled to a microstrip SM1 and the gate of Q1 at one end and to receive the gate bias voltage (vg1) from the bias control circuit 10. As such, R1 of Matsunaga is coupled, at one end, to a microstrip and a gate of a transistor Q1 – not an IC pin - and, at the other end, to a bias control circuit – not a return voltage -.

The Examiner further states that a second IC pin coupled to receive analog signals from a source is shown in Figure 6 by elements 71-85, which receives analog signals from 80. Claim 1 claims a second IC pin operably coupled to receive analog signals from a microphone, not a multitude of components that receive analog signal from a source. Again, the Examiner seems to be equating an IC to an IC pin.

The Examiner yet further states that at least one off-chip component couples the second IC pin to the first IC pin is disclosed in Figure 5 via Pout and Vapc. Firstly, Figure 5 is a graph that plots operating current Id verses output power Pout. [See column 10, lines 58-63.] Secondly, Vapc is discussed with reference to Figure 7 as a power control signal voltage. [See column 11, lines 62-63.] Thus, Pout is a measure of power and Vapc is a control signal, not an off-chip component coupled between first and second IC pins as is presently claimed.

Claim 1 further includes the limitation that the variable supply voltage buffer provides the buffered supply voltage to second IC pin as a microphone bias voltage. The

Examiner does not address this limitation. Nevertheless, the Matsunaga reference does not render obvious such as a limitation.

Based on the foregoing discussion, the applicant contends that Matsunaga has been misinterpreted with respect to claim 1 and, as such, combining the teachings of Matsunaga with Aubauer fails to render claim 1 obvious since Matsunaga does not teach of suggest the elements of a microphone bias circuit as demonstrated above.

Claims 2-6 are dependent upon claim 1 and introduce additional patentable subject matter. The applicant believes that the reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claims 2-6 over the same rejection.

The applicant believes that the reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claims 8 over the same rejection.

3. Claims 7 and 9-14 have been rejected under 35 USC § 103 (a) as being unpatentable over Matsunaga (U.S. Patent No. 6,759,906) in view of Aubauer (U.S. Patent Application No. US2005/0276423) and Melo (U.S. Patent No. 6,243,817). The applicant respectfully disagrees with this rejection and the reasoning thereof.

The applicant believes that, since Matsunaga fails to teach or suggest elements of the microphone bias circuit, the reasons that distinguish claim 1 over its rejection are applicable in distinguishing claims 7 and 9-14 over their respective rejections.

For the foregoing reasons, the applicant believes that claims 1-14 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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